AMENDMENTS TO THE CLAIMS

Please cancel claims 3-11 without prejudice or disclaimer, and add new claims 12-33, to read as follows

1. (Original) An annealed wafer obtained by performing heat treatment on a silicon wafer manufactured from a silicon single crystal grown by the Czochralski method, wherein a good chip yield of an oxide film dielectric breakdown characteristic in a region having at least a depth of up to 5 μm from a wafer surface is 95% or more, and a density of oxide precipitates detectable in the wafer bulk and each having a size not smaller than a size showing a gettering capability is not less than $1 \times 10^9/cm^3$.

2. (Original) The annealed wafer according to claim 1, wherein the silicon wafer is manufactured from a silicon single crystal grown under a condition that, when growing the silicon single crystal, a wafer entire surface is an N region which is formed outside an OSF generated in the form of a ring in a thermal oxidation process, and is free from a defective region detectable by a Cu deposition method.

3-11. (Cancelled)

12. (New) The annealed wafer according to claim 1, wherein the silicon wafer is manufactured from a silicon single crystal grown without adding nitrogen when growing the silicon single crystal.

13. (New) The annealed wafer according to claim 2, wherein the silicon wafer is manufactured from a silicon single crystal grown without adding nitrogen when growing the silicon single crystal.

14. (New) A method for manufacturing an annealed wafer comprising the steps of: manufacturing a silicon wafer from a silicon single crystal obtained by growing the silicon single crystal under controlling a growth rate between a first growth rate at a boundary where a defective region left after annihilation of an OSF ring and detectable by a Cu deposition method is annihilated when the growth rate of pulling a silicon single crystal is gradually reduced, and a second growth rate at a boundary where an interstitial dislocation loop is generated when the growth rate is further gradually reduced in case of growing the silicon single crystal by a Czochralski method; keeping the silicon wafer having grown-in precipitation nuclei formed in the step of growing the silicon single crystal at a temperature of T_4°C in the range of 500°C to 700°C for a predetermined time t_1; increasing the temperature of the silicon wafer to a temperature of T_5°C in the range of 1000°C to 1230°C with a temperature increase rate of 5°C/min or less; and keeping the silicon wafer at the temperature of T_5°C for a predetermined time t_2, whereby the grown-in precipitation nuclei are grown to oxide precipitates each having a size not smaller than a size having a gettering capability and oxygen in the vicinity of the silicon wafer surface is outdiffused.

15. (New) The method for manufacturing an annealed wafer according to claim 14, wherein the keeping time t_1 at the temperature of T_4°C is 15 minutes or more.

16. (New) The method for manufacturing an annealed wafer according to claim 14, wherein the keeping time t_2 at the temperature of T_5°C is 30 minutes or more.

17. (New) The method for manufacturing an annealed wafer according to claim 15, wherein the keeping time t_2 at the temperature of T_5°C is 30 minutes or more.

18. (New) A method for manufacturing an annealed wafer comprising the steps of: manufacturing a silicon wafer from a silicon single crystal obtained by growing the silicon single crystal under controlling a growth rate between a first growth rate at a boundary where a defective region left after annihilation of an OSF ring and detectable by a Cu deposition method is annihilated when the growth rate of pulling a silicon single crystal is gradually reduced, and a second growth rate at a boundary where an interstitial dislocation loop is generated when the growth rate is further gradually reduced in case of growing the silicon single crystal by a Czochralski method; and heat treating the silicon wafer having grown-in precipitation nuclei formed in the step of growing the silicon single crystal to give a getting capability to the silicon wafer, wherein there are performed at least three steps including a temperature increase step A_1 for growing the grown-in precipitation nuclei, a temperature increase step B_1 for increasing a temperature to a higher keeping temperature, and a constant-temperature keeping step C_1 for growing the grown-in precipitation nuclei to oxide precipitates each having a size not smaller than a size having a gettering capability and for outdiffusing oxygen in the vicinity of the silicon wafer surface.

19. (New) The method for manufacturing an annealed wafer according to claim 18, wherein the temperature increase step A_1, the temperature increase step B_1, and the constant-temperature keeping step C_1 are continuously performed.

20. (New) The method for manufacturing an annealed wafer according to claim 18, wherein the temperature increase step A_1 is for increasing a temperature from T_6°C to T_7°C at a rate of R_3°C/min, T_6°C is 700°C or less, T_7°C is in the range of 800°C to 1000°C, and R_3°C/min is 3°C/min or less.

21. (New) The method for manufacturing an annealed wafer according to claim 19, wherein the temperature increase step A_1 is for increasing a temperature from T_6°C to T_7°C at a rate of R_3°C/min, T_6°C is 700°C or less, T_7°C is in the range of 800°C to 1000°C, and R_3°C/min is 3°C/min or less.

22. (New) The method for manufacturing an annealed wafer according to claim 18, wherein before increasing the temperature from T_6°C to T_7°C in the temperature increase step A_1, the temperature of T_6°C is kept for 30 minutes or more.

23. (New) The method for manufacturing an annealed wafer according to claim 19, wherein before increasing the temperature from T_6°C to T_7°C in the temperature increase step A_1, the temperature of T_6°C is kept for 30 minutes or more.

24. (New) The method for manufacturing an annealed wafer according to claim 20, wherein before increasing the temperature from T_6°C to T_7°C in the temperature increase step A_1, the temperature of T_6°C is kept for 30 minutes or more.

25. (New) The method for manufacturing an annealed wafer according to claim 21, wherein before increasing the temperature from T_6°C to T_7°C in the temperature increase step A_1, the temperature of T_6°C is kept for 30 minutes or more.

26. (New) The method for manufacturing an annealed wafer according to claim 18, wherein the temperature increase step B_1 is for increasing the temperature from T_7°C to T_8C at a rate of R_4°C/min, T_7°C is in the range of 800°C to 1000°C, T_8°C is in the range of 1050°C to 1230°C, and R_4°C/min is 5°C/min or more.

27. (New) The method for manufacturing an annealed wafer according to claim 19, wherein the temperature increase step B_1 is for increasing the temperature from T_7°C to T_8C at a rate of R_4°C/min, T_7°C is in the range of 800°C to 1000°C, T_8°C is in the range of 1050°C to 1230°C, and R_4°C/min is 5°C/min or more.

28. (New) The method for manufacturing an annealed wafer according to claim 20, wherein the temperature increase step B_1 is for increasing the temperature from T_7°C to T_8C at a rate of R_4°C/min, T_7°C is in the range of 800°C to 1000°C, T_8°C is in the range of 1050°C to 1230°C, and R_4°C/min is 5°C/min or more.

29. (New) The method for manufacturing an annealed wafer according to claim 21, wherein the temperature increase step B_1 is for increasing the temperature from T_7°C to T_8C at a rate of R_4°C/min, T_7°C is in the range of 800°C to 1000°C, T_8°C is in the range of 1050°C to 1230°C, and R_4°C/min is 5°C/min or more.

30. (New) The method for manufacturing an annealed wafer according to claim 22, wherein the temperature increase step B_1 is for increasing the temperature from T_7°C to T_8C at a rate of R_4°C/min, T_7°C is in the range of 800°C to 1000°C, T_8°C is in the range of 1050°C to 1230°C, and R_4°C/min is 5°C/min or more.

31. (New) The method for manufacturing an annealed wafer according to claim 23, wherein the temperature increase step B_1 is for increasing the temperature from T_7°C to T_8C at a rate of R_4°C/min, T_7°C is in the range of 800°C to 1000°C, T_8°C is in the range of 1050°C to 1230°C, and R_4°C/min is 5°C/min or more.

32. (New) The method for manufacturing an annealed wafer according to claim 24, wherein the temperature increase step B_1 is for increasing the temperature from T_7°C to T_8C at a rate of R_4°C/min, T_7°C is in the range of 800°C to 1000°C, T_8°C is in the range of 1050°C to 1230°C, and R_4°C/min is 5°C/min or more.

33. (New) The method for manufacturing an annealed wafer according to claim 25, wherein the temperature increase step B_1 is for increasing the temperature from T_7°C to T_8C at a rate of R_4°C/min, T_7°C is in the range of 800°C to 1000°C, T_8°C is in the range of 1050°C to 1230°C, and R_4°C/min is 5°C/min or more.